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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,116	03/30/2001	Michael N. Derr	219.39308X00	3264

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EXAMINER	
PRIETO, BEATRIZ	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,116	DERR, MICHAEL N.	
	Examiner	Art Unit	
	Prieto Beatriz	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Application No. 09/821,116 filed March 30, 2001, claims 1-19 have been examined.

2. Regarding claims 3-4, 9-10, 14-15, 18 and 19 and the use of acronyms IDE & DMA, it is respectfully suggested to spell-out this acronym where it initially appears. Base claims 1, 12, and 16 have "overwritten" mis-spelled, correction is required.

Claim Rejection under 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,999,441 RUNALDUE et. al. (Runaldue).

Regarding claim 1, Runaldue teaches substantial features of the invention, including

writing individual bits of data to a "register" memory (10) (col 1/lines 14-17, 60-64 and col 2/lines 51-56), said method comprising:

receiving bits of input data in a data field (DATA [0:7]) to be stored in said register, the register composed of memory cells (12) arranged in eight columns [0:7] (14), thereby the number of bits in said input data field being equal to the number of bits in the register and bit locations in the data field corresponding respectively to "bit locations" addresses in the register (Fig. 1, and col 3/lines 30-57);

receiving enable bits in a bit enable field (BIT_EN) from logic (18), the number of enable bits in the bit enable field being equal to the number of bits in the register and "bit locations" addresses in the bit enable field corresponding respectively to "bit locations" addresses in the register (col 3/lines 65-col 4/line 5, col 5/lines 28-29 and col 1/lines 19-41), and

overwriting only the bits at the bit locations of the register according to the write enable bits in the write enable field (WRTDAT) for which the enable bit in the corresponding location in the bit

enable field is set with the bit of input data in the corresponding location in the data field (col 2/lines 7-12, 20-32).

Claim Rejection under 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12-19 and 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,567,953 Pomerantz in view of Runaldue.

Regarding claim 12, Pomerantz teaches a computer system (100 of Fig. 1) comprising:

a processor subsystem (101); a device (13) which exchange data bi-directionally with said processor subsystem (Fig. 2);

a controller (131 or 111) connected between said device and said processor subsystem (Fig. 2), said controlled executing a method comprising; said controller further comprising (controller 140 of Fig. 2) adapted to control the transfer of data between said device and said processor subsystem (col 4/lines 43-col 6/line 2), however Pomerantz does not teach the method performed by said controller as described on claim 12;

Runaldue teaches receiving bits of input data in a data field (DATA [0:7]) to be stored in said register, the register composed of memory cells (12) arranged in eight columns [0:7] (14), thereby the number of bits in said input data field being equal to the number of bits in the register and bit locations in the data field corresponding respectively to "bit locations" addresses in the register (Fig. 1, and col 3/lines 30-57);

receiving enable bits in a bit enable field (BIT_EN) from logic (18), the number of enable bits in the bit enable field being equal to the number of bits in the register and "bit locations" addresses in the bit enable field corresponding respectively to "bit locations" addresses in the register (col 3/lines 65-col 4/line 5, col 5/lines 28-29 and col 1/lines 19-41), and

overwriting only the bits at the bit locations of the register according to the write enable bits in the write enable field (WRTDAT) for which the enable bit in the corresponding location in the bit enable

field is set with the bit of input data in the corresponding location in the data field (col 2/lines 7-12, 20-32).

It would have been obvious to one ordinary skilled in the art at the time the invention was made given the suggestion of Runaldue for applying the his teachings to application using random access memory for storing data having multiple configuration lengths, the applicability to Pomerantz environment including PC cards, i.e. memory cards, e.g., a SRAM (Static Random Access Memory) card, ROM (Read Only Memory) card, Flash Memory card (i.e. rewritable), etc., an ATA (AT attachment) card for functioning as a hard disk with an IDE (Integrated Drive Electronics) interface, a FAX (facsimile) card, typically used for communicating via telephone lines, a LAN card for connecting PCs via LAN, a SCSI (Small Computer System Interface) card for connecting to a SCSI apparatus, a sound card for playing music or producing sound effects by a PC, an ISDN (Integrated Services Digital Network) card for connecting to ISDN lines, and a Video Capture card for capturing a video signal. Motivation to combine would be modify data, such as individual bits of an addressed word within a single clock, reducing latency.

Regarding claim 13, an interconnecting device/means "bridge" 131 between the processor subsystem and at least said device, the controller being included in the bridge (Pomerantz: Fig. 1).

Regarding claim 14, wherein the device comprises an IDE storage device (137) and the bridge comprises an "I/O controller hub" (ICH) which controls an IDE data transfer between the processor subsystem and the IDE storage device (Pomerantz: col 4/lines 23-31).

Regarding claim 15, this claim is substantially the same as claim 10, same rationale of rejection is applicable.

Regarding claim 16, this claim comprises the software program stored in a tangible medium, said program, when executed, causing a computer to execute a method of claim 1, discussed above, same rationale of rejection is applicable.

Regarding claim 17, wherein said software program comprises a driver in the operating system software executed by a processor subsystem in the computer (Pomerantz: col 1/lines 65-col 2/line 5).

Regarding claims 18-19, this claim is substantially the same as combined limitations claims 1-3, and 9-10, same rationale of rejection is applicable

Regarding claims 2-3, wherein the register is a control register for a data transfer operation (Pomerantz: col 8/lines 44-col 9/line 2), including transfers data to or from an IDE storage device (Pomerantz: Fig. 2).

Regarding claims 4-5, wherein the control register is an "IDE DMA" status register (Pomerantz: col 1/lines 54-col 2/line 2 and col 4/lines 23-42), and wherein the control register is a command register (Pomerantz: col 8/line 44-col 9/line 2).

Regarding claims 6-8, wherein some of the bits of said register are not overwritten (Runaldue: col 2/lines 25-32), wherein the data field and the bit enable field are received in parallel (Runaldue; col 2/lines 14-25) and wherein the data field is provided at an address which is contiguous with the address for the bit enable field (Runaldue: 7-bit address signal (ADDR) [0:7] of Fig. 1, i.e. continuous).

Regarding claim 9, wherein the data transfer operation comprises an IDE data transfer between a processor subsystem and an external IDE storage device (137) (Runaldue: Fig. 2).

Regarding claim 10, wherein the processor subsystem (host) posts an entire command sequence for setting up the IDE data transfer (col 5/lines 5-20).

Regarding claim 11, wherein the method is carried out in an IDE controller in a interconnecting device or means "bridge" (131) connected between the processor subsystem and the external IDE storage device or peripheral (Pomerantz: Fig. 2).

Pertinent Prior Art:

7. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure; pertinence is presented in accordance with MPEP§ 707.05. Copies of Non-Patent Literature documents cited will be provided as set forth in MPEP§ 707.05(a):

U.S. 6,598,157

McKee teaches the computer of claim 12, including a processor subsystem (102, 110, 103), a device (124) which transfer data to/or from said processor subsystem; and a controller (130) connected between said device and said processor subsystem and adapted to control the transfer of data between said device and said processor subsystem; said controller including a interconnecting device/means "bridge" I/O controller hub which controls an IDE data transfer between the processor subsystem and the IDE storage device (124).

U.S. 6,704,808

Kasamatsu et. al. discloses a PCI bus 20 and the ISA bus 22 are interconnected through a multifunctional PCI device 38, device 38 provides a bridge function between the PCI bus 20 and the ISA bus 22, a Direct Memory Access (DMA) controller function, a Programmable Interrupt Controller (PIC) function, a Programmable Interval Timer (PIT) function, an Integrated Drive Electronics (IDE) interface function, a Universal Serial Bus (USB) function, and a System Management Bus (SMB) interface function, and may be a PIIX4 device from Intel Corporation, for example. EEPROM 50 is also connected to the multifunctional PCI device 38 through an SM bus. The EEPROM 50 holds information such as a password registered by a user, a supervisor password, and a product serial number, is non-volatile, and its content is electronically rewritable.

U.S. 5,752,075

Kikinis teaches a bus 101, connects to includes a scanner drive controller and interface circuit 91 and a printer drive controller and interface circuit 93, and provides parallel data communication with circuits that are typical and well-known in current PC art, such as a random access memory (RAM) 79, a super video- graphics array (SVGA) display adapter 81, a keyboard controller 83, a serial port 11, a parallel port 9, a floppy disk controller (FDC) 89, an integrated electronics disk (IDE) controller 95, a mouse port 5, and a personal computer memory card international association (PCMCIA) slot 15, and the like.

US 5,980,276

Arita, et. al. teaches wherein among the PC cards, there are a memory card, e.g., a SRAM (Static Random Access Memory) card, ROM (Read Only Memory) card, Flash Memory card, etc., an ATA (AT attachment) card for functioning as a hard disk with an IDE (Integrated Drive Electronics) interface, a FAX (facsimile) card for communicating via telephone lines, a LAN (Local Area Network) card for connecting PCs via LAN, a SCSI (Small Computer System Interface) card for connecting to a SCSI apparatus, a sound card for playing music or producing sound effects by a PC, an ISDN (Integrated Services Digital Network) card for connecting to ISDN lines, and a Video Capture card for capturing a video signal.

U.S. 4,153,950

Nosowicz teaches a register array comprises a plurality of shift registers, each having 16-bit storage cells writable in parallel groups simultaneously, data can be recorded in these storage cells from the bit selector only when a cell row such as cells 0-3 or 4-7 are gated by address decode circuit 25. Data bytes (i.e. 16 binary bits) for storage within array 20 are retrieved from a character generator or other

source and transmitted first to the 19-bit shift register 22 as a succession of single bytes. A data byte retrieved from the character generator is transmitted in parallel to the first 16 bit positions of the 19-bit shift register 22

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prieto, B. whose telephone number is (571) 272-3902. The Examiner can normally be reached on Monday-Friday from 6:00 to 3:30 p.m. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, Jack B. Harvey can be reached on (571) 272-3896. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800/4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system, status information for published application may be obtained from either Private or Public PAIR, for unpublished application Private PAIR only (see http://pair-direct.uspto.gov or the Electronic Business Center at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

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or faxed to the Central Fax Office:

(703) 872-9306, for Official communications and entry;

Or Telephone:

(703) 306-5631 for TC 2100 Customer Service Office.

B. Prieto
TC 2100
Patent Examiner
February 16, 2005

Beatriz Prieto
Patent Examiner